

By

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## SUMMARY

A phased array module has been designed containing a matched power divider and four 3-bit phase shifter channels, each of which has a 3 dB splitter and two 180 degree phase shifter bits. In this way, 3-bit phase control is accomplished along with electronic switching between two radiative polarizations on both transmit and receive.

Three thousand modules (containing 12000 phase shifters) have been completed for use in a phased array antenna. Each phase shifter channel was tested using a Hewlett-Packard 1000 automated network analyzer. Average insertion loss of less than 1.7 dB (after allowance for power division) was realized with 13 degrees RMS error for the entire 12000 phase shifter assembly. This insertion loss includes the ohmic dissipation in the absorptive 8 to 1 overall power division inherent in the module's design as well as ohmic and reflective losses of a push-on simultaneous connection of the eight RF output ports of the module.

Special considerations encountered in the design, manufacture and automated measurement of these modules will be highlighted in the talk.

## INTRODUCTION

To build large electronically steered phased array antennas it is useful to incorporate some of the array power division within the phase shifter modules. In this way some economy of production is realized by incorporating, for example, 4 phase shifters in a common housing. At the same time a 4 to 1 power division is achieved which eliminates what would otherwise be a connector interface between the array power divider network and 4 individual phase shifter channels. Such a scheme was described for an L-band module [Ref. 1, 2]. This paper describes an extension to S-band of that approach and the practical design manufacture and measurement results obtained from a run of over 3,000 such modules. Other new results include the provision for dual RF polarizations through the use of an extra 180 degree phase shift bit in each channel, the first production usage of an RF connector rail which makes 8 phase precise, simultaneous push-on connections, and built-in logic to provide "row and column" steering capability within the modules.

## RF CIRCUIT

A schematic diagram of the RF circuit is shown in Figure 1. The incident RF power is divided using a 4 to 1 splitter that consists of two tiers of 3 dB coupler power dividers with two important features.

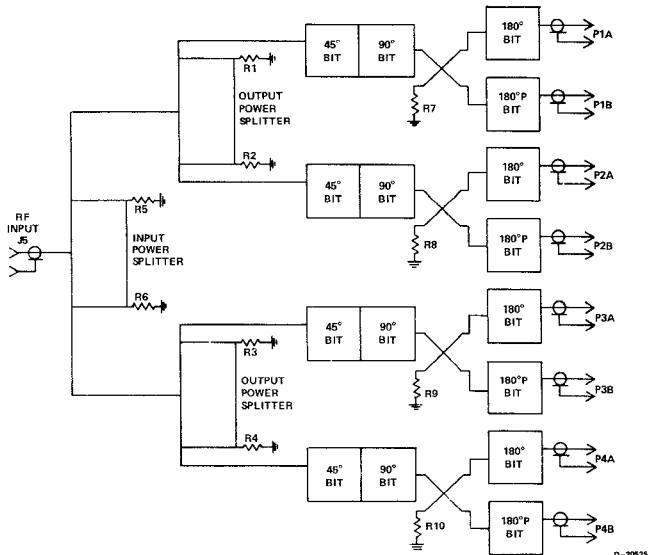


FIGURE 1 RF CIRCUIT LAYOUT

First, matched loads absorb phase asymmetric reflected energy from the antenna radiating elements. In this way, large VSWR encountered at off axis scan angles is damped. Unlike Wilkinson dividers, these couplers use two separate loads for each 2 to 1 split. Not only does this double power absorption capability for a given load power rating but, more importantly, less insertion loss at  $f_0$  because the loads are in a voltage standing wave null when the divider is operating under matched conditions.

A photograph showing the RF side of the module is shown in Figure 2. As can be seen the divider network is realized in air dielectric stripline and the phase shifter channels, each of which consists of one 45, one 90, and two 180 degree bits (driven by a built-in 3 dB quadrature coupler) is realized in solid TFG dielectric.

This module has been designed as a standard series (MA-8360-16SLD) for use in the 2.5 to 3.5 GHz frequency band. The cen-

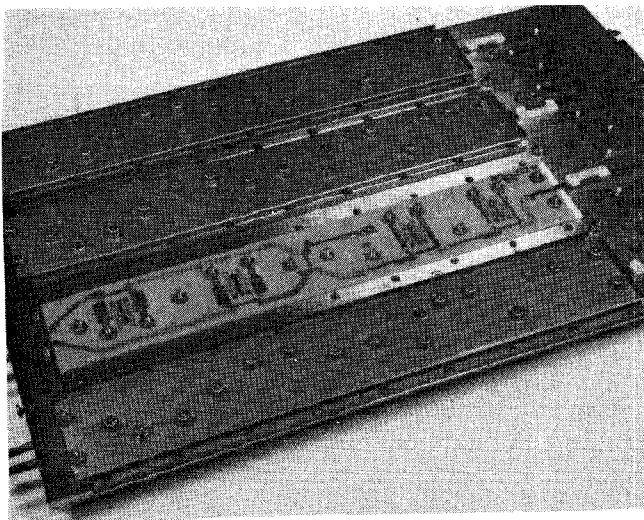


FIGURE 2 DUAL POLARIZED PHASE SHIFTER SUBASSEMBLY

ter frequency for each application is adjusted by scaling of the circuit dimensions to the particular application center frequency; about 10% bandwidth is thereby achieved.

High power testing is performed on every production module using a sliding short circuit termination system which subjects all phase shifter channels to the maximum encounterable voltage and current stresses. The power rating depends somewhat upon the specific operating frequency and pulse length but typically one kilowatt per channel (4 kilowatts per module) peak power, 50 watts of average power with up to 500 microsecond evenly spaced RF pulses is achievable. Special, 50 ohm, beryllia base ceramic loads were made for the assembly which are capable of absorbing the full reflected power under any phasing conditions.

The eight RF output connectors, 2 for each of the 4 channels may be seen in Figure 3, which also shows the opposite side of the assembly, containing the driver and logic circuitry. These RF connectors are electrically similar to the standard 3 mm SMA connector except that they are designed for a push on installation and were furnished by Amphenol, Inc. They are built into a strong brass rail which serves as the aligning and mounting surface for the module. For flexibility the connectors are attached via 2 inch lengths of 0.18 inch diameter copper coaxial line. The mating connectors have a bell shaped outer connector to guide and straighten the output lines. The lengths of all output connectors were held precisely to 0.005 inch tolerance for precise output phase and amplitude matching under the constraint of their simultaneous connections. This connector interface is reproducible to within 0.05 dB of insertion loss and 2 degrees of RF phase variation. To our knowledge, no major phased array system constructed at this high a frequency range has demonstrated the use of such a connector system, which allows for plugging the module directly into the rear face of the array antenna.

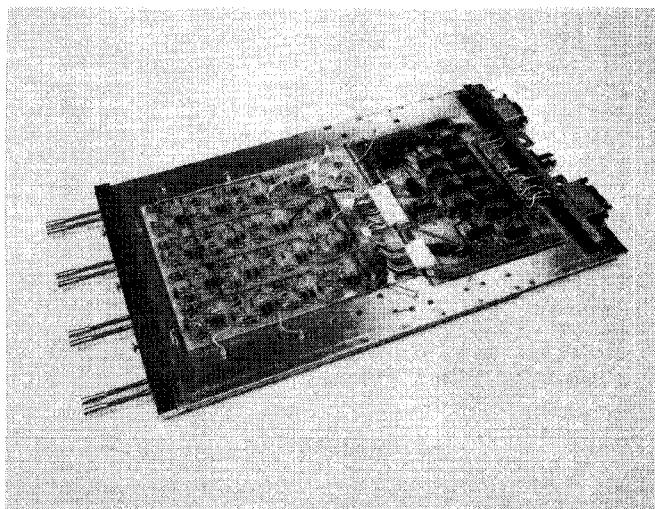


FIGURE 3 LOGIC-DRIVER ASSEMBLY  
DRIVER AND LOGIC

Four separate drivers each using a 2 transistor set to drive each phase shifter bit can be seen in Figure 3. All of the drivers were built on a single board measuring approximately 8 X 10 inches and interconnected to a second logic board via board connectors. Design of the drivers followed typical practice [Ref. 2, Chapter 4] transistors are stressed at no more than one half of their breakdown voltage, for reliable operation. Negative 30 volts at 36 mA maximum reverse bias and +3.6 amperes maximum at +4 volts of total forward bias, is supplied to the entire module. An additional +5 volts at +525 mA maximum is required for the logic. In order to safeguard against operation of the assembly under high RF power excitation without bias, interlock pins are located in the bias connectors. These are wired to an array interlock mechanism which inhibits the application of RF high power when an open circuit (disconnected bias connector) is detected.

The logic circuit shown is built up using 15 standard logic circuit modules. The detailed description of the logic circuit schematic diagram is beyond the scope of this summary, but it's function is as follows. Simultaneous "row" and "column" commands are applied to the bias connector using serial four bit words. The logic sums these two words and rounds off (drops two pi multiples) to determine the actual phase command needed for each particular phase channel. This operation is performed four times sequentially for the four channels. The commands are then stored in the logic until an "enable" command is applied, at which time all phase shifters in the array antenna assume the new phase commands and the beam of the antenna is thereby shifted.

Through use of this row and column steering, individual wires between the beam steering computer and the phase shifters need not be run. Rather, all rows of the antenna are wired to "row" busses and all columns to "column" busses. Each individual assembly is connected to the appropriate in-

tersection of such busses and thereby derives its own unique commands. Not only is wiring saved, but, by incorporating the row and column addition within the phase shifter module, a portion of the beam steering logic effectively is realized within the module, thereby reducing the amount of computation and storage capability needed within the beam steering computer.

Over 3000 modules were made and tested. Insertion loss was less than 2.5 dB peak and 1.7 dB average, RMS phase shift error was below 12 degrees. The balance between dual polarization channels was within 0.5 dB in amplitude and 5 degrees in phase.

#### REFERENCES

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2. J. F. White, MICROWAVE SEMICONDUCTOR ENGINEERING, Van Nostrand Rheinhold, N.Y., 1981 (previously entitled SEMICONDUCTOR CONTROL, Artech Publishers).

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